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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Andrew Marshall

Docket No.: TI-31484

Serial No.: 10/007,332

Art Unit: 2815

Filed: 11/08/01

Examiner: Warren, M. E.

Title: Thermal Coupling of Matched SOI Device Bodies

APPELLANT'S BRIEF UNDER 37 CFR 1.192

December 15, 2004

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)

I hereby certify that the above correspondence is being deposited with the U.S. Postal Service on 12-15-04 as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Karen Vertz 12-15-04

Karen Vertz Date

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Pursuant to the Advisory Action mailed 09/20/2004, the Appellant submits this Appellant's Brief in triplicate. The Commissioner is hereby requested and authorized to charge any fees necessary for the filing of the enclosed papers to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation.

RELATED APPEALS AND INTERFERENCES

No related appeals or interferences are known to the Appellant.

STATUS OF CLAIMS

Claims 6-13 and 15-19 are the subject of this appeal. Claims 1-13 and 15-19 are pending; Claims 1-5 stand allowed, and Claims 6-13 and 15-19 are rejected.

STATUS OF AMENDMENTS

The Appellant filed an amendment under 37 C.F.R. § 1.111 on May 12, 2004 in response to the office action dated February 17, 2004.

The Appellant filed another amendment under 37 C.F.R. § 1.116 on August 30, 2004 in response to the final action dated July 26, 2004. This amendment did not contain any proposed claim changes.

SUMMARY OF THE INVENTION

Independent Claim 6 is directed to a semiconductor-on-insulator ("SOI") circuit structure (page 1 lines 6-9). The SOI circuit comprises a pair of transistors in an analog circuit stage which requires the matched behavior of the transistor pair (page 8 lines 16-18, FIG. 5). There is a physical connection of metallic material which provides thermal conduction between respective bodies of the pair of transistors (page 8 lines 20-22, FIG. 5), and an insulating layer beneath the transistor pair (page 1 lines 10-12, page 5 lines 14-20). There is also an insulating barrier substantially surrounding the pair and extending to the insulating layer (page 5 lines 14-17, page 8 lines 22-25, FIG. 5).

Claim 7 is dependent on Claim 6 and further specifies that the analog circuit stage is a current mirror (page 7 lines 9-10, page 8 lines 18-22, FIG. 5).

Claim 8 is dependent on Claim 6 and further specifies that the analog circuit stage is a matched pair of current-sourcing P-channel transistors in a current mirror (page 8 lines 18-22, FIG. 5).

Claim 9 is dependent on Claim 6 and further specifies that the physical connection comprises metal interconnects between the transistors of the transistor pair (page 8 line 21, FIG. 5).

Independent Claim 10 is directed to a SOI circuit structure (page 1 lines 6-9). The SOI circuit comprises a plurality of matched transistors in an analog circuit stage which requires matched behavior of the transistors (page 7 lines 17-18). The respective bodies of the transistors are formed from different semiconductor sections, the sections being formed on an insulating layer and at least partially separated by insulating material (page 7 lines 20-22, FIG. 3, page 3 lines 1-5, page 5 lines 14-20). In addition, the bodies are not tied to any fixed potential through a low impedance path (FIG. 3, page 1 lines 11-12, page 2 lines 1-3) and the bodies are thermally coupled by a connection of non-insulating material (page 7 lines 22-25, FIG. 3, page 3 lines 1-5, page 5 lines 11-13).

Claim 11 is dependent on Claim 10 and further specifies that the bodies are electrically coupled by a connection of non-insulating material (FIG. 3, page 7 lines 22-25).

Claim 12 is dependent on Claim 10 and further specifies that the analog circuit stage is a current mirror (FIG. 3, page 7 lines 16-18).

Claim 13 is dependent on Claim 10 and further specifies that the connection of non-insulating material is made from semiconductor material (FIG. 3, page 7 lines 22-25).

Claim 15 is dependent on Claim 10 and further specifies that the analog circuit stage is a matched pair of current-sourcing P-channel transistors in a current mirror (FIG. 3, page 7 lines 15-18).

Independent Claim 16 is directed to a method of circuit operation (page 8 line 26 to page 9 line 17). The method comprises providing a pair of matched transistors in a circuit stage which requires matched behavior of the transistor pair (FIG. 6, page 9 line 3), providing a physical connection of material which provides thermal conduction between respective bodies of the pair of transistors (page 9 lines 12-14), and surrounding the circuit stage with an insulating material (FIGS. 6-6a, page 9 lines 18-20).

Claim 17 is dependent on Claim 16 and further specifies that the physical connection is of a semiconductor material (page 9 lines 4-14).

Claim 18 is dependent on Claim 16 and further specifies that the circuit stage is an analog circuit stage (FIG. 6, page 14 lines 3-4).

Claim 19 is dependent on Claim 16 and further specifies that the physical connection does not carry current during normal operation of the circuit stage (page 9 lines 8-9 and 12).

ISSUES

1. Whether Claims 10-15 are unpatentable under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement.

2. Whether Claims 6, 9, and 16-19 are unpatentable under 35 U.S.C. §102(a) over the patent granted to Flaker et al. (U.S. Pat. No. 6,133,608).

3. Whether Claims 10-13 and 15 are unpatentable under 35 U.S.C. §102(a) over the patent granted to Houston et al. (U.S. Pat. No. 6,037,808).

4. Whether Claims 7 and 8 are unpatentable under 35 U.S.C. §103(a) over the patents granted to Flaker et al. (U.S. Pat. No. 6,133,608) and further in view of Houston et al. (U.S. Pat. No. 6,037,808).

GROUPING OF CLAIMS

Claims 6-13 and 15-19 stand separately.

ARGUMENT

Issue 1 - Whether Claims 10-15 are unpatentable under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement.

The Appellant respectfully traverses the 35 U.S.C. §112, second paragraph rejection of Claim 1 since the Appellant specifically states on page 1 line 12 that the "transistor body is typically left floating". On page 3 line 13, the Appellant specifically states that disclosed methods and structures have "electrical isolation from external sources".

The Appellant respectfully traverses the statement in the Office Action that "It seems that if a source or drain is tied to a fixed potential, then the body of the transistor is also tied to a fixed potential." The Appellant submits that, while it may seem that the body may be tied to a fixed potential, in practice the body is in an area of opposite diffusion type (i.e. n-type or p-type) to the source and drain. As a result, when there is a single connection to the source or drain the entire silicon mesa tends, in the DC condition, to be at the same potential; therefore, the device would have no use (and would have no impact on the total circuit). However, when a second (different) potential is applied to the drain, the body will attain its own potential - which will vary depending on the rate of change of the voltage on the other pins (i.e. drain, gate, and source) and the temperature (which will modify leakage). The Appellant respectfully submits that this is in no way equivalent to being tied to a fixed potential.

Therefore, Claims 10-15 are patentable under 35 U.S.C. §112, first paragraph.

Issue 2 - Whether Claims 6, 9, and 16-19 are unpatentable under 35 U.S.C. §102(a) over the patent granted to Flaker et al. (U.S. Pat. No. 6,133,608).

Claim 6 positively recited a pair of transistors in an analog circuit stage which requires matched behavior of the transistor pair. In addition, Claim 6 positively recites a physical connection of metallic material which provides thermal conduction between respective bodies of a pair of transistors. These advantageously claimed features are not taught or suggested by the patent granted to Flaker et al.

The Appellant respectfully traverses the indication in the Office Action (page 8) that "In fact, metals naturally have the properties of electrical conduction and thermal conduction. Because Flaker teaches the use of metal to provide an electrical link between transistors, then Flaker inherently teaches that link provides thermal conduction." The Appellant agrees that metals have both thermal and electrical properties; however, the Appellant submits that metals in configurations having good electrical conduction don't necessarily have good thermal properties. For example, if heat dissipated strongly down metal wires, then the wires of an electric space heater would get hot through conduction from the element – which they clearly do not.

The Appellant respectfully traverses the indication in the Office Action (bottom of page 3) that Flaker et al. teaches, in column 6 line 53 through column 7 line 4, a physical connection of metallic material for a pair of transistors in an analog circuit stage. The Appellant submits that Flaker et al. is discussing a digital application (column 6 lines 56-59, column 7 lines 3-4) that may use a metal link instead of silicon. Arguably this implies that Flaker et al. does not comprehend the use of metal links in SOI analog circuit stages.

The Appellant notes that in FIG. 10B (referenced in the Office Action on page 3) that Flaker et al. teaches the addition of an extra oxide layer (40) that would reduce the thermal coupling (column 5 lines 49-55); and therefore teaches away from providing thermal conduction between respective bodies of the pair of transistors as advantageously claimed.

The Appellant respectfully traverses the indication in the Office Action (twice on page 3) that Flaker et al. teaches thermal conduction. The Appellant submits that Flaker et al. merely teaches equilibration of the body charge differentials due to thermal effects (column 4 lines 60-67); which is entirely different than equalizing the thermal effects (i.e. is less efficiently equalized in Flaker's partial trench scheme than in a scheme that does not constrict the conductive silicon height).

Therefore, Claim 6 is patentable over the patent granted to Flaker et al.

Claim 9 is dependent on Claim 6 and is therefore allowable for the same reasons that Claim 6 is allowable. Furthermore, Claim 9 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 6, are not taught nor suggested by the patent granted to Flaker et al. Namely, Claim 9 further specifies the additional limitation that the physical connection comprises metal interconnects between the transistors of the transistor pair.

In addition, the Appellant traverses the indication in the Office Action (top of page 4) that Flaker et al. teaches a physical connection of metallic material that provides thermal conduction between transistors. The Appellant submits that Flaker et al.'s metal link provides electrical conduction (column 7 lines 1-4), not thermal conduction as advantageously claimed.

Therefore, Claim 9 is patentable over the patent granted to Flaker et al.

Claim 16 positively recites a physical connection of material which provides thermal conduction between respective bodies of a pair of transistors. These advantageously claimed features are not taught or suggested by the patent granted to Flaker et al.

The Appellant respectfully traverses the indication in the Office Action (page 8) that "In fact, metals naturally have the properties of electrical conduction and thermal conduction. Because Flaker teaches the use of metal to provide an electrical link between transistors, then Flaker inherently teaches that link provides thermal conduction." The Appellant agrees that metals have both thermal and electrical properties; however, the Appellant submits that metals in configurations having good electrical conduction don't necessarily have good thermal properties.

In addition, the Appellant submits that Flaker et al. merely teaches equilibration of the body charge differentials due to thermal effects (column 4 lines 60-67); which is entirely different than equalizing the thermal effects (i.e. is less efficiently equalized in Flaker's partial trench scheme than in a scheme that does not constrict the conductive silicon height).

The Appellant respectfully traverses the indication in the Office Action (page 4) that Flaker et al. teaches thermal conduction. The Appellant submits that Flaker et al. merely teaches equilibration of the body charge differentials due to thermal effects (column 4 lines 60-67); which is entirely different than equalizing the thermal effects (i.e. is less efficiently equalized in Flaker's partial trench scheme than in a scheme that does not constrict the conductive silicon height).

The Appellant notes that if Flaker et al. had been discussing thermal connectivity then he would not have formed a more thermally resistive silicon link – which is what is being done by the addition of the extra process step that he is using to get the so called 'partial trench'.

The Appellant also notes that in the application shown in FIG. 10B that Flaker et al. teaches the addition of an extra oxide layer (40) that would reduce the thermal coupling (column 5 lines 49-55); and therefore teaches away from providing thermal conduction between respective bodies of the pair of transistors as advantageously claimed.

Therefore, Claim 16 is patentable over the patent granted to Flaker et al.

Claim 17 is dependent on Claim 16 and is therefore allowable for the same reasons that Claim 16 is allowable. Furthermore, Claim 17 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 16, are not taught nor suggested by the patent granted to Flaker et al. Namely, Claim 17 further specifies the additional limitation that the physical connection is of a semiconductor material.

Therefore, Claim 17 is patentable over the patent granted to Flaker et al.

Claim 18 is dependent on Claim 16 and is therefore allowable for the same reasons that Claim 16 is allowable. Furthermore, Claim 18 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 16, are not taught nor suggested by the patent granted to Flaker et al. Namely, Claim 18 further specifies the additional limitation that the circuit stage is an analog circuit stage.

As noted in the Office Action on page 4, "Flaker et al. does not specifically disclose that the circuit stage is an analog stage." The Appellant submits that Flaker et al. does not provide any enabling description of the use of Flaker's circuit in an analog circuit stage.

Therefore, Claim 18 is patentable over the patent granted to Flaker et al.

Claim 19 is dependent on Claim 16 and is therefore allowable for the same reasons that Claim 16 is allowable. Furthermore, Claim 19 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 16, are not taught nor suggested by the patent granted to Flaker et al. Namely, Claim 19 further specifies the additional limitation that the physical connection does not carry current during normal operation of the circuit stage.

The Appellant respectfully traverses the indication in the Office Action (page 4) that Flaker et al. implies that the body link (32) that does not carry current during normal

operation of the circuit. The Appellant submits that Flaker et al.'s intrinsic silicon bridge (despite a high resistance) will still conduct electricity (though it may indeed be a poor conductor compared to highly doped silicon). Flaker et al. even states that an electrically conductive bridge is formed (column 5 lines 1 and 4).

Therefore, Claim 19 is patentable over the patent granted to Flaker et al.

Issue 3 - Whether Claims 10-13 and 15 are unpatentable under 35 U.S.C. §102(a) over the patent granted to Houston et al. (U.S. Pat. No. 6,037,808).

Claim 10 positively recites that transistor bodies are thermally coupled by a connection of non-insulating material. These advantageously claimed features are not taught or suggested by the patent granted to Houston et al.

Houston et al. does not teach a physical connection that provides thermal conduction between respective bodies of transistors as advantageously claimed. Rather, Houston et al. teaches electrical conduction between two transistors (column 4 lines 25-28, column 9 lines 35-42; column 17 lines 20-37). The Appellant submits that configurations having good electrical conduction don't necessarily have good thermal properties. Houston et al. does not teach providing thermal conduction between respective bodies of a pair of transistors in an analog circuit stage as advantageously claimed.

Therefore, Claim 10 is patentable over the patent granted to Houston et al.

Claim 11 is dependent on Claim 10 and is therefore allowable for the same reasons that Claim 10 is allowable. Furthermore, Claim 11 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 10, are not taught nor suggested by the patent granted to Houston et al. Namely, Claim 11 further specifies the additional limitation that the bodies are electrically coupled by a connection of non-insulating material.

Therefore, Claim 11 is patentable over the patent granted to Houston et al.

Claim 12 is dependent on Claim 10 and is therefore allowable for the same reasons that Claim 10 is allowable. Furthermore, Claim 12 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 10, are not taught nor suggested by the patent granted to Houston et al. Namely, Claim 12 further specifies the additional limitation that the analog circuit stage is a current mirror.

Therefore, Claim 12 is patentable over the patent granted to Houston et al.

Claim 13 is dependent on Claim 10 and is therefore allowable for the same reasons that Claim 10 is allowable. Furthermore, Claim 13 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 10, are not taught nor suggested by the patent granted to Houston et al. Namely, Claim 13 further specifies the additional limitation that the connection of non-insulating material is made from semiconductor material.

Therefore, Claim 13 is patentable over the patent granted to Houston et al.

Claim 15 is dependent on Claim 10 and is therefore allowable for the same reasons that Claim 10 is allowable. Furthermore, Claim 15 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 10, are not taught nor suggested by the patent granted to Houston et al. Namely, Claim 15 further specifies the additional limitation that the analog circuit stage is a matched pair of current-sourcing P-channel transistors in a current mirror.

Therefore, Claim 15 is patentable over the patent granted to Houston et al.

Issue 3 - Whether Claims 7 and 8 are unpatentable under 35 U.S.C. §103(a) over the patents granted to Flaker et al. (U.S. Pat. No. 6,133,608) and further in view of Houston et al. (U.S. Pat. No. 6,037,808).

Claim 7 is dependent on Claim 6 and is therefore allowable for the same reasons that Claim 6 is allowable. Furthermore, Claim 7 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 6, are not taught nor suggested by the patents granted to Flaker et al. and Houston et al.; either alone or in combination. Namely, Claim 7 further specifies the additional limitation that the analog circuit stage is a current mirror.

The Appellant respectfully traverses the assertion in the Office Action (page 6) that it would have been obvious to "...modify the matched transistor pair of Flaker by incorporating a current mirror..." The Appellant submits that the teaching of Flaker et al. are not sufficient for use in an analog circuit stage, including the analog circuit of Houston et al. In addition, the Appellant submits that combining two patents that don't teach a 'physical connection of metallic material which provides thermal conduction between respective bodies of a transistor pair' won't render obvious the Appellants advantageously claimed 'physical connection of metallic material which provides thermal conduction between respective bodies of a transistor pair.'

Therefore, Claim 7 is patentable over the patents granted to Flaker et al. and Houston et al.; either alone or in combination.

Claim 8 is dependent on Claim 6 and is therefore allowable for the same reasons that Claim 6 is allowable. Furthermore, Claim 8 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 6, are not taught nor suggested by the patents granted to Flaker et al. and Houston et al.; either alone or in combination. Namely, Claim 8 further specifies the additional limitation that the analog circuit stage is a matched pair of current-sourcing P-channel transistors in a current mirror.

The Appellant respectfully traverses the assertion in the Office Action (page 6) that it would have been obvious to "...modify the matched transistor pair of Flaker by incorporating a current mirror..." The Appellant submits that the teaching of Flaker et al. are not sufficient for use in an analog circuit stage, including the analog circuit of Houston et al. In addition, the Appellant submits that combining two patents that don't teach a 'physical connection of metallic material which provides thermal conduction between respective bodies of a transistor pair' won't render obvious the Appellants advantageously claimed 'physical connection of metallic material which provides thermal conduction between respective bodies of a transistor pair.'

Therefore, Claim 8 is patentable over the patents granted to Flaker et al. and Houston et al.; either alone or in combination.

ADDITIONAL ARGUMENTS

In response to the additional comments on page 2 of the Advisory Action the Appellant reiterates the following points. The Appellant specifically states on page 1 line 12 that the "transistor body is typically left floating." In addition, the Appellant specifically states that the disclosed methods and structures have "electrical isolation from external sources" (page 3 line 13).

As shown in FIGS. 3-6a, the body is in an area of opposite diffusion type (i.e. n-type or p-type) to the source and drain. As a result, when there is a single connection to the source or drain the entire silicon mesa tends, in the DC condition, to be at the same potential; therefore, the device would have no use (and would have no impact on the total circuit). However, when a second (different) potential is applied to the drain, the body will attain its own potential - which will vary depending on the rate of change of the voltage on the other pins (i.e. drain, gate, and source) and the temperature (which will modify leakage).

Furthermore, while the Appellant agrees that metals have both thermal and electrical properties, the Appellant submits that metals in configurations having good electrical conduction don't necessarily have good thermal properties. For example, if heat dissipated strongly down metal wires, then the wires of an electric space heater would get hot through conduction from the element – which they clearly do not.

CONCLUSION

For the reasons stated above, the Appellants respectfully contend that each claim is patentable. Therefore, the reversal of all rejections is courteously solicited.

Respectfully submitted,

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APPENDIX

Claims on Appeal

6. An integrated circuit semiconductor-on-insulator circuit structure, comprising:

a pair of transistors in an analog circuit stage which requires matched behavior of said pair;

a physical connection of metallic material which provides thermal conduction between respective bodies of said pair of transistors; and

an insulating layer beneath said pair;

an insulating barrier substantially surrounding said pair and extending to said insulating layer.

7. The integrated circuit of Claim 6, wherein said analog circuit stage is a current mirror.

8. The integrated circuit of Claim 6, wherein said analog circuit stage is a matched pair of current-sourcing P-channel transistors in a current mirror.

9. The integrated circuit of Claim 6, wherein said physical connection comprises metal interconnects between said transistors of said pair.

10. An integrated semiconductor-on-insulator circuit structure, comprising:

a plurality of matched transistors in an analog circuit stage which requires matched behavior of said transistors;

wherein respective bodies of said transistors are formed from different semiconductor sections, said sections being formed on an insulating layer and at least partially separated by insulating material;

wherein said bodies are not tied to any fixed potential through a low impedance path; and

wherein said bodies are thermally coupled by a connection of non-insulating material.

11. The integrated circuit of Claim 10, wherein said bodies are electrically coupled by a connection of non-insulating material.

12. The integrated circuit of Claim 10, wherein said analog circuit stage is a current mirror.

13. The integrated circuit of Claim 10, wherein said connection of non-insulating material is made from semiconductor material.

15. The integrated circuit of Claim 10, wherein said analog circuit stage is a matched pair of current-sourcing P-channel transistors in a current mirror.

16. A method of circuit operation, comprising the steps of:

providing a pair of matched transistors, in a circuit stage which requires matched behavior of said pair; and

providing a physical connection of material which provides thermal conduction between respective bodies of said pair of transistors; and

surrounding said circuit stage with an insulating material.

17. The method of Claim 16, wherein said physical connection is of a semiconductor material.

18. The method of Claim 16, wherein said circuit stage is an analog circuit stage.

19. The method of Claim 16, wherein said physical connection does not carry current during normal operation of said circuit stage.